Designing of a 10MHz BW 77dB SNDR 8.1mW Continuous-Time Delta-Sigma Modulator With a Proposed Low Power, Rail-to-Rail Output Swing OPAMP

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Abstract The design of a single-loop 4th order 10MHz bandwidth, 320MHz sampling frequency (OSR=16) continuous-time delta-sigma is presented. This design is intended to minimize the power consumption in a low-voltage environment. A low power, low noise complimentary input OPAMP, the most power-consumed block in the modulator, is proposed in this design. As a result, the modulator achieves a simulated peak SNDR of 77dB in a 10MHz bandwidth, consumes 8.1mW at 1.2V supply voltage, and occupies an area of 900µm x 480µm in a standard 90nm CMOS process.

Keyword Continuous-time Delta-Sigma modulator, low power, rail-to-rail operational amplifier

1. Introduction

ΔΣ analog-to-digital converters have become very popular in recent years as they can provide high resolution and low power data conversion. Among the ΔΣ converters, discrete-time (DT) modulators are less suitable for high-speed conversions because settling time requirements boost their power consumption. Therefore, they are used for high-accuracy conversions within lower bandwidths [1,2]. Besides higher sampling rates, continuous-time (CT) converters; on the other hand, have additional advantages over DT modulators: no sample-and-hold in front, an inherent anti-aliasing filter generation by the filter circuits. Recent CMOS implementations show feasible input bandwidths up to a few tens MHz [3,4].

The key features of realizing low power, high resolution ΔΣ modulator, both in discrete-time and continuous-time, are lowering the power consumption of the operational amplifier (OPAMP), the most power-consumed block in the modulator. It leads to minimize the input transconductance g_m of the OPAMP as much as possible, which can increase the input-referred noise. For the first integrator, where no noise shaping takes place, the problem will become more critical and decrease the resolution of the modulator. To overcome these problems, a low power, low noise complimentary input OPAMP is proposed. Comparing with conventional Opamp using either NMOS input or PMOS input, for the same drain current, the proposed one has double power efficiency according to double of the input transconductance. Moreover, the proposed OPAMP shows the best noise characteristic. Hence, low-power, high resolution ΣΔ modulator can be realized easily.

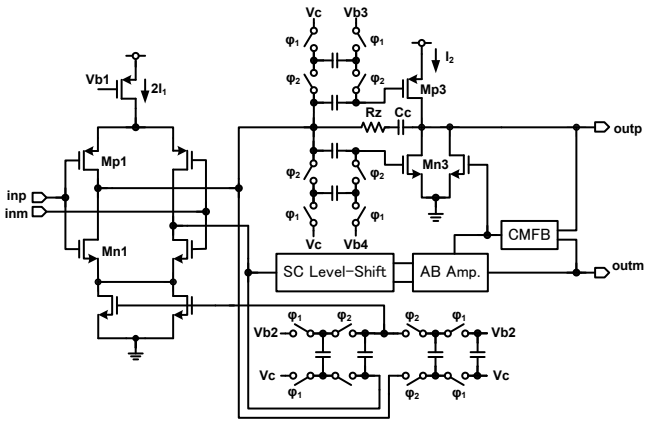

Fig.1. The proposed OPAMP schematic

This paper is structured as follows: In Sect. 2, the proposed OPAMP will be presented and analyzed. In Sect. 3, we describe an implementation of a 4th order, 10 MHz bandwidth CT ΣΔ modulator using the proposed OPAMP. In Sect. 4, the simulated performance of that modulator will be shown. In Sect. 5, we end up with some conclusions.

2. Proposed OPAMP

The OPAMP composes the main building block of the ΔΣ modulator. The requirements for the OPAMP are mainly output swing, dc gain, and gain bandwidth (GBW). The output swing is very important in low voltage design because it determines the maximum input amplitude as well as the dynamic range of the modulator. Fig. 1 shows the schematic of our proposed two-stage OPAMP with complimentary input in the first stage to achieve low power, low noise characteristic and class-AB buffer in the

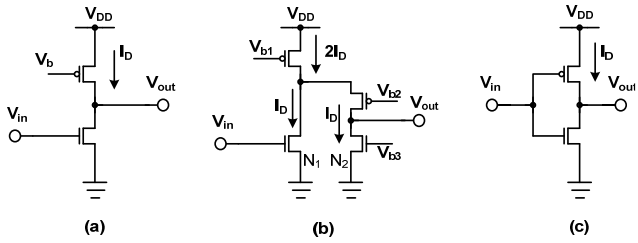

Fig.2. Model of noise analyzation: (a) common-source, (b) folded-cascode and (c) complimentary

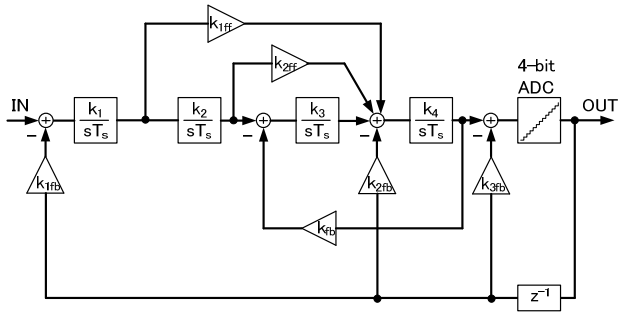

Fig.3. Continuous-time ΣΔ modulator architecture.

second stage for rail-to-rail output swing. The phase margin is compensated according to Miller compensation capacitance C_c. They will be explained in detail in the next section.

2.1. Low noise, low power

For a given *GBW* and load capacitance C_L, the required input transconductance can be calculated as

$$g_m = 2\pi \cdot GBW \cdot C_c \tag{1}$$

where C_c is Miller compensation capacitance. Due to complimentary input, for the same drain current I_{D1}, the g_m of proposed OPAMP increases by 2, and double power efficiency can be achieved.

$$g_m = g_{mN1} + g_{mP1} \tag{2}$$

$$g_{mN1} = g_{mP1} = \frac{2I_{D1}}{V_{eff}} \tag{3}$$

where $V_{eff} = V_{GSmN1} - V_{THn} = V_{GSmP1} - V_{THp}$ is the overdrive voltage of the input transistors.

Besides that, the complimentary input architecture also shows the best noise characteristic. To simplify the calculation, three single-ended basic types of OTAs: common-source, folded-cascode and complimentary are modeled to analyze (Fig. 2). Assume that the drain currents and overdrive voltages of all input transistors are same in three cases. Therefore, the input-referred noise

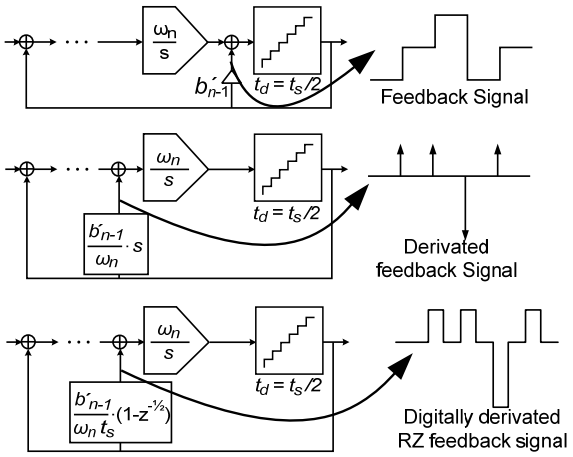

Fig.4. Realization of the zero order quantizer feedback path [6].

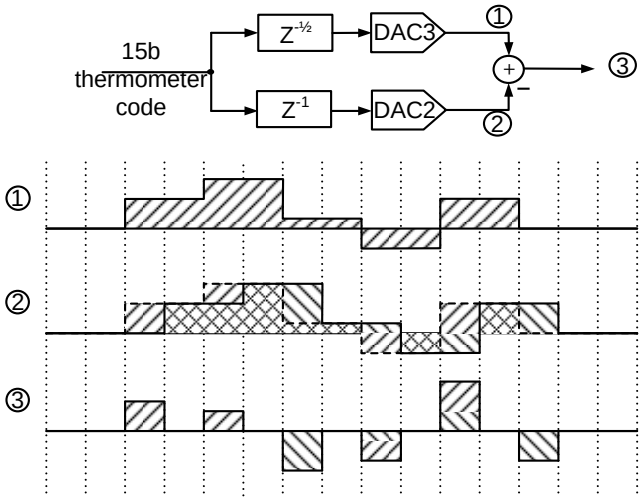

Fig.5. Generation of the RZ pulse shaped time-discrete differentiated feedback signal [6].

can be approximately estimated as follows

*Common-source

$$\overline{v_{n,in}^2} \approx 4kT\gamma\left(\frac{1}{g_{mn}} + \frac{g_{mp}}{g_{mn}^2}\right) \approx 2 \times \frac{4kT\gamma}{g_{mn}} \tag{4}$$

*Folded-cascode

$$\overline{v_{n,in}^2} \approx 4kT\gamma\left(\frac{1}{g_{mn1}} + \frac{g_{mn2}}{g_{mn1}^2} + 2 \cdot \frac{g_{mp}}{g_{mn1}^2}\right) \approx 4 \times \frac{4kT\gamma}{g_{mn}} \tag{5}$$

*Complimentary

$$\overline{v_{n,in}^2} \approx 4kT\gamma \frac{g_{mn} + g_{mp}}{\left(g_{mn} + g_{mp}\right)^2} \approx \frac{1}{2} \times \frac{4kT\gamma}{g_{mn}} \tag{6}$$

Here k is Boltzmann constant, k=1.38x10-23 J/K, T is the absolute temperature in degrees Kelvin, γ is noise coefficient, γ=2/3 for long-channel transitor and larger value for submicron MOSFETs. We define noise figure of merit of a circuit as the product of input-referred noise

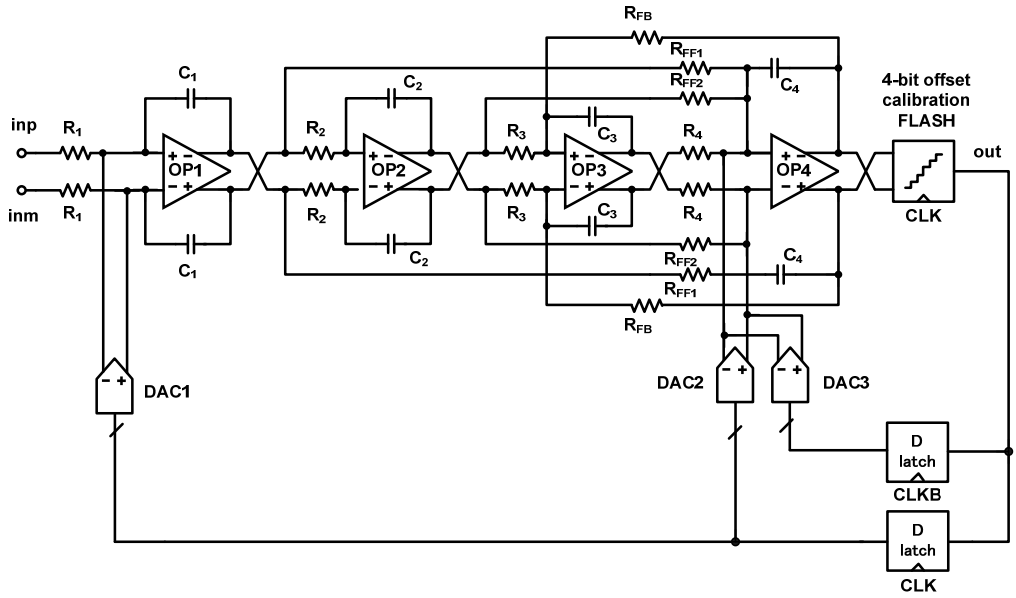

Fig.6. 4th order, 4-bit continuou-time ΣΔ modulator.

power and its operating current which can be described briefly as follows:

$$FoM_{noise} = \frac{1}{4kT}\overline{v_{n,in}^2} I_D \quad (7)$$

As a result, the noise figure of merit of three OTAs can be derived as

*Common-source

$$FoM_{noise} = \frac{1}{4kT} \cdot 2 \times \frac{4kT\gamma}{g_{mn}} \cdot I_D = \gamma \frac{2I_D}{g_{mn}} = \gamma V_{eff} \quad (8)$$

*Folded-cascode

$$FoM_{noise} = \frac{1}{4kT} \cdot 4 \times \frac{4kT\gamma}{g_{mn}} \cdot 2 \times I_D = 4\gamma V_{eff} \quad (9)$$

*Complimentary

$$FoM_{noise} = \frac{1}{4kT} \cdot \frac{1}{2} \times \frac{4kT\gamma}{g_{mn}} \cdot I_D = \frac{1}{4}\gamma V_{eff} \quad (10)$$

where V_{eff} is the overdrive voltage of the input transistors. From (8)~(10) we can realize that the complimentary architecture have the best noise performance, up to 16 times smaller when comparing with the folded-cascode architecture.

2.2. Rail-to-rail output swing

As described above, the maximum output swing of OPAMP is required to increase the maximum input amplitude as well as the dynamic range of the modulator. In low voltage environment, the rail-to-rail output swing for the OPAMP is highly preferred, and the class-AB output stage satisfies this requirement. Higher slew rate can be obtained from the class-AB output stage with less power consumption. In [5], an implementation of the class-AB biasing is described, but it seems difficult to keep all the transistors to work in the saturation region in the corner conditions. Hence, a switched-capacitor level shifter is applied to bias the class-AB output stage in our proposed OPAMP, as shown in Fig. 1. The corner simulation was done to verify all the transistors to work in the saturation region.

3. Building block circuits

3.1. Topology consideration

Our goal is to realize a 10 MHz bandwidth, 13 bit resolution CT ΣΔ modulator with minimum power consumption at 1.2V supply-voltage in a standard 90nm CMOS process. In order to save the power, architectures with low over-sampling ratios (OSRs) are preferable for a signal bandwidth of 10 MHz. To suppress quantization noise sufficiently for 13 bit performance, multibit quantization and at least a third-order noise-transfer function (NTF) are essential.

The proposed CT ΣΔ modulator architecture is shown in Fig. 3. The modulator comprises a 4-bit internal quantizer, operating at 320 MHz with an oversampling ratio of 16, and a forth-order single-loop filter. In order to maintain a good alias filter characteristic, a combination of feedforward and feedback stabilized loop filter is implemented [5] (see Fig. 3). The delay of 4-bit quantizer is set to one of the sampling period. This large delay is

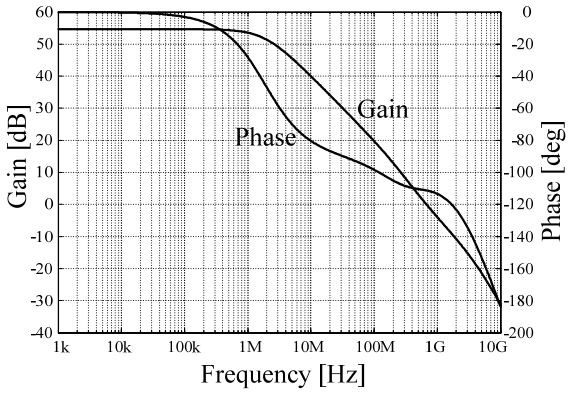

Fig.7. Simulated OPAMP frequency response.

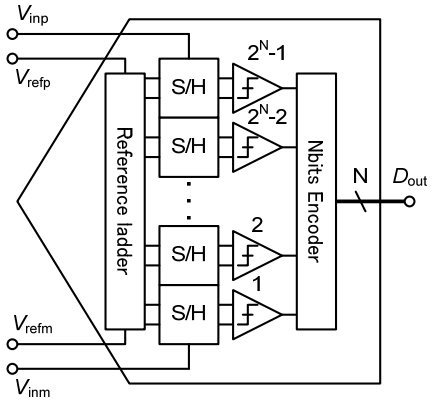

Fig.8. Four-bit quantizer

compensated exactly by an additional feedback path (see Fig. 3). To relax the sum circuit before the quantizer, a differentiation operation in the direct feedback path k_{3fb} is introduced, as shown in Fig 4. It is realized at circuit level as follow: the discrete time differentiation is carried out by subtracting from the feedback signal 1of DAC3, a delayed version, signal 2, that is output by DAC2 half a clock period later (Fig. 5). In effect, signal 3 is proportional to the derivative of the quantizer output, and has RZ pulse shaping. Applying to our designed modulator, the full circuit level can be achieved as shown in Fig. 6, where all feedback DACs (DAC1, DAC2 and DAC3) are designed as NRZ ones.

3.2. OPAMPs

The simulated frequency response of the proposed OPAMP in Sect. 2 with 5.2-pF and 3.75-kΩ load is depicted in Fig. 7. The gain reaches 55 dB and the GBW is 700 MHz while the phase margin is kept at 68 degrees, with a power consumption of 1.8 mW.

According to one of the most interesting property of ΣΔ modulators, the noise suppression inside the loop, the

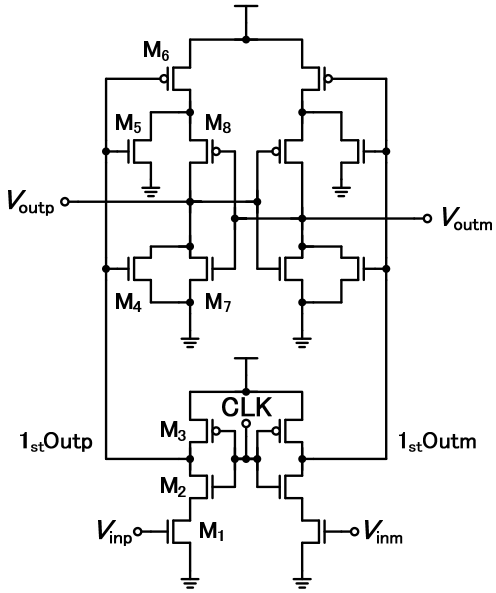

Fig.9. Double-tail latch comparator

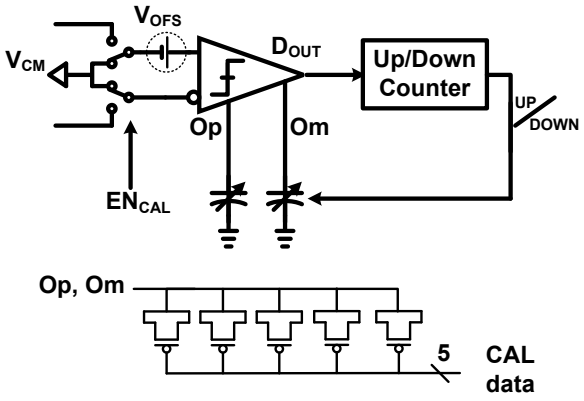

Fig.10. Comparator offset calibration

load of the second integrator is scaled down. Reduction of the load capacitance, hence, reduces the power consumption of the OPAMP. The second OPAMP with 1.25-pF and 2.27-kΩ load consumes 0.9mW. The scaling is also applied for the third and forth integrator. As a result, the total power consumption of four OPAMPs is 4.5 mW.

3.3. Quantizer

The quantizer in the modulator (Fig. 8) consists of a reference ladder and a 4-bit flash ADC with a thermometer-coded output that is sampled by the latches of the current-steering DAC. The 15 comparators of the internal flash ADC are realized with a double tail latch and a SR latch, shown in Fig. 9 [7].

During the reset phase, while CLK is low, nodes Op and Om are precharged to supply voltage V_{DD}. After reset phase, while CLK goes high, at nodes Op and Om, the

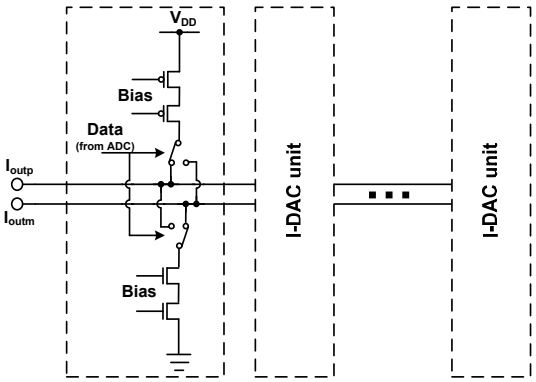

Fig. 11. Current-steering DAC architecture

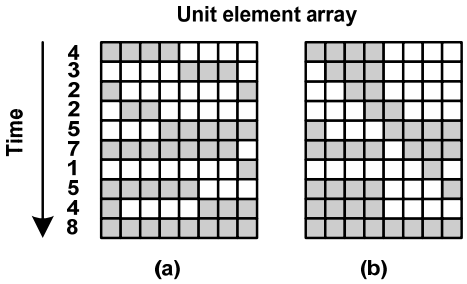

Fig.12. Element rotation algorithm for an eight-element DAC: (a) convetional pattern and (b)1 element pattern

common-mode voltage drops and an input dependent differential voltage ΔV_O will build up in a short time. The proposed comparator uses the falling edge at the Op and Om nodes for the latch timing of the second stage. The result is then latched by the SR latch following. The whole comparator is a pure dynamic circuit, which is very power efficient.

As shown in Fig. 10, the calibration architecture for the offset voltage cancellation of the comparator consists of a comparator, an updown counter and two 5 bit digital varactors [7]. The loop filter is disconnected during calibration and the input stages are connected to the common-mode voltage, providing zero differential input voltage to all comparator inputs. The digital varactors are controlled so that Op and Om should fall at the same speed. The digital varactors are composed of 5 bit binary weighted PMOS array. The offset variation is reduced from 10 mV_{RMS} to 1.3 mV_{RMS}, obtained from Spectre Monte Carlo 100 times simulation.

3.4. Feedback DAC

As described in Sect. 3.1, for one clock delay compensation and differentiation operation in the direct feedback path, a third DAC operating on a clock CLKB,

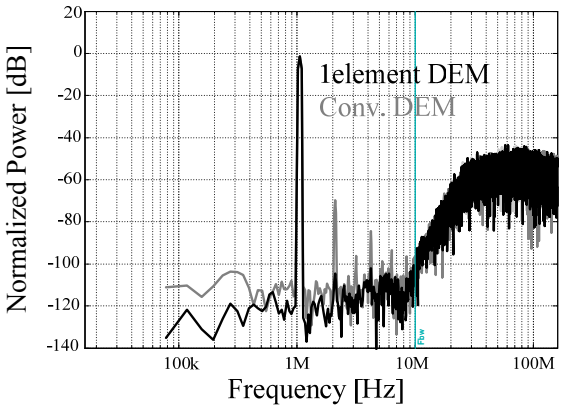

Fig.13. Performance comparison with 0.7% DAC1 mismatch

delayed by half a sampling period, is required. DAC1 realizes an input to the loop filter and, hence, has the highest requirements on linearity and noise performance, which requires a large device size to get the necessary matching and flicker noise performance. As any nonidealities of DAC2 and DAC3 are suppressed by the gain of the first three integrators, the requirements on noise and linearity can be relaxed. All DACs are cascoded to increase their output resistance and shield the large drain capacitance of the current-source transistors from the tail node of the switches, as shown in Fig. 11.

3.5. Dynamic Element Matching (DEM)

Besides using the large device, a DAC linearization technique, Dynamic Element Matching (DEM) is also applied to achieve better linearity performance. The DEM technique is not free from limitations, however. It needs considerable amount of time to execute the algorithm and this timing problem is more critical in a high-speed continuous-time ΣΔ modulator. In order to minimize the quantization-to-DAC delay, a low-latency DEM with switch matrix is applied [9]. Therefore, an element rotation scheme can be adopted for its simplicity and potential to move DEM outside the loop.

Fig. 12 shows an example of element rotation algorithm for an eight-element DAC. By alternately choosing each element of the DAC, the average DAC output matches the ideal mean value. In the traditional pattern, all the DAC elements should be used at the maximum possible rate while ensuring that each element is used the same number of times. This is done by sequentially selecting elements from an array, beginning with the next available unused element, as shown in Fig. 12(a). But in that case the number of elements that changes its state every time data is input will be increased, leading to the increasing of the

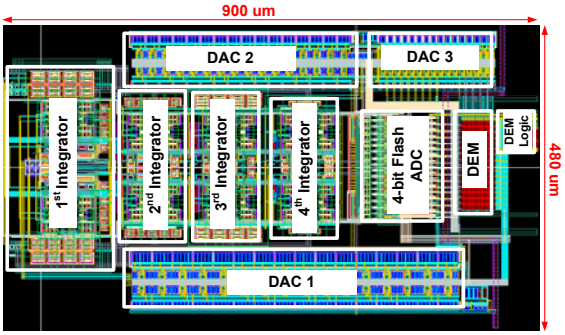

Fig.14. Layout of the modulator

DAC output glitch. As a result, unwanted harmonics appear and decrease the resolution of the modulator, as can be seen in Fig 13. In order to overcome this problem but still remain the characteristic of DEM, we proposed a 1 element pattern DEM in Fig. 12(b). With this proposed DEM, the number of state-changed elements will be kept smaller when comparing with the conventional DEM. The simulation result using our proposed DEM is shown in Fig. 13 and good performance (resolution) can be achieved.

4. Simulated Performance

The chip was fabricated in a standard digital 90-nm CMOS technology. The power supply voltage was 1.2 V and the reference voltage was 1.0 V. The chip core size was 900 µm x 480 µm, as illustrated in Fig. 14. This design achieved 77.9 dB resolution (Fig. 14) and consumed 8.1 mW. The performance of this design, comparing with recent published paper is summarized in Table 1.

5. Conclusion

A low power, low noise complimentary input OPAMP has been proposed. Due to that proposed OPAMP, a low power, high resolution ΣΔ modulator can be realized in a low voltage environment easily. By proper topology selection and proposed 1 element pattern DEM, the modulator achieved a simulated peak SNDR of 77dB in a 10MHz bandwidth, consumes 8.1mW at 1.2V supply voltage, and occupies an area of 900µm x 480µm in a standard 90nm CMOS process.

Acknowledgement

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References

[1] Y. Chae, I. Lee and G. Han, "A 0.7V 36µW 85dB-DR Audio ΔΣ Modulator Using Class-C Inverter," *ISSCC Dig. Tech. Papers*, pp. 490-491, Feb. 2008.

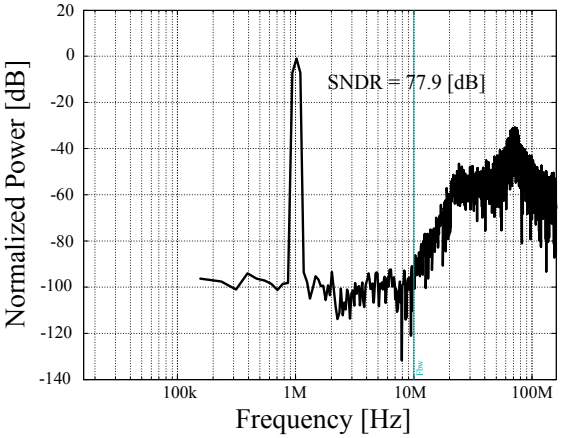

Fig.15. Simulated performance (all transitor level)

Table 1. Simulated performance comparing with recent puslished papers.

SNDR [dB]	Power [mW]	FoM [pJ/conv]	BW [MHz]	Fs [MHz]	Supply [V]	Reference
77	**8.1**	**0.07**	**10**	**320**	**1.2**	**This work (SIM)**
74	20	0.12	20	640	1.2	ISSCC 2006 3.1
72	28	0.22	20	420	1.2	ISSCC 2008 27.5
66	7.5	0.23	10	600	1.8	ISCAS 2006
62.5	5.32	0.24	10	300	1.1	VLSI 2009
60	10.5	0.32	20	250	1.3	ISSCC 2009 9.7
78.1	87	0.33	20	900	1.5	ISSCC 2009 9.5
68.8	42.6	0.41	23	276	1.8	ISSCC 2005 27.6
79	75	0.43	12	240	2.5	ISSCC 2003 23.6
82	100	0.49	10	640	1.8	ISSCC 2008 27.6
69	56	0.61	20	340	1.2	ISSCC 2007 13.1

[2] H. Park, K. Nam, D. K. Su, K. Vleugels and B. A. Wooley, "A 0.7V 100dB 870µW Digital Audio ΣΔ Modulator," *IEEE Symp. on VLSI Circuits*, pp. 178-179, Jun. 2008.

[3] G. Mitteregger *et al.*, "A 20-mW 640-MHz CMOS Continuous-Time ΣΔ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, Vol. 41, No. 12, pp. 2641-2649, Dec. 2006.

[4] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho and A. Matsuzawa, "A 5th-Order Delta-Sigma Modulator with Single-Opamp Resonator," *IEEE Symp. on VLSI Circuits*, pp. 68-69, Jun. 2009.

[5] A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio ΔΣ Modulator with 98dB Dynamic Range," *ISSCC Dig. Tech. Papers*, pp. 50-51, Feb. 1999.

[6] L.Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-µW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, Vol. 39, No. 11, pp. 1809-1818, Nov. 2004.

[7] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," *ASSCC Dig. Tech. Papers*, pp. 269-272, Nov. 2008.

[8] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx,"An 820µW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp.238-239, Feb. 2008.

[9] S. J. Huang and Y. Y. Lin,"A 1.2V 2MHz BW 0.084mm^2 CT ΔΣ ADC with -97.7dBc THD and 80dB DR Using Low-latency DEM," *ISSCC Dig. Tech. Papers*, pp.172-173, Feb. 2009.